J Electroceram (2010) 25:174–178
DOI 10.1007/s10832-010-9612-9

Characterization of Au/Pb($Zr_{0.96}Ti_{0.04}$)O_3/Al_2O_3/Si antiferroelectric field-effect transistors for memory application

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Received: 2 February 2010 / Accepted: 19 May 2010 / Published online: 8 June 2010
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Abstract Polarization-voltage (*P-V*) hysteresis loops and polarization retention were studied for Au/Pb($Zr_{0.96}Ti_{0.04}$)O_3/Al_2O_3/Pt antiferroelectric capacitors with different Al_2O_3 layer thicknesses. The high-field ferroelectric phase after poling can be pertained to zero external field with the choice of an appropriate Al_2O_3 layer thickness. At the same time, a strong depolarization field across the Al_2O_3 layer is generated with the direction opposite to the field across the Pb($Zr_{0.96}Ti_{0.04}$)O_3 layer. The depolarization-field direction can be reversed with the domain switching of the high-field ferroelectric phase, possessing the potential application of antiferroelectric memories. A large memory window of 10 V was observed for Au/Pb($Zr_{0.96}Ti_{0.04}$)O_3 (50 nm)/ Al_2O_3 (6.3 nm)/n-Si (100) field-effect transistors, as confirmed from the capacitance sweeping under voltages between −19 and +19 V. The high/low capacitance ratio is over 8:1, and the ratio remains stable with time over 4 h after programming voltage of ±19 V at 80°C, in suggestion of the excellent retention of the memory.

Keywords Ferroelectric phase stabilization · Antiferroelectric memories · Memory window · Data retention

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1 Introduction

Ferroelectric random access memories have attracted considerable attentions in past years for the advantages of low power consumption, fast writing/reading speed, and cell size scalability for high-density memories [1–7], among which the metal/ferroelectric/ insulator/semiconductor field-effect transistor (FeFET) shows excellent characteristics of non-destructive readout and integrating compatibility with standard CMOS process. However, the data retention, which is one of most important issues for memory commercialization, is still poor for this kind of memory due to some material inefficiencies, such as the formation of high-density interface traps and charge injection into the ferroelectric film, which increases the leakage current to eliminate the depolarization field [8–11].

To enhance the memory retention, the high-k materials such as Al_2O_3 [12], Si_3N_4 [13], $LaAlO_3$ [14], HfO_2 [15–17], HfAlO [18, 19], CeO_2 [20], MgO [21], Dy_2O_3 [22], Y_2O_3 [23, 24], HfTaO [25], etc., have been used as a buffer layer between ferroelectric and semiconductor layers to reduce ionic interdiffusion and interfacial charge trapping. So far to now, the retention is not satisfied yet, since the memory window is maintained only for a few days, far shorter from the 10-year requirement. This is a major barrier to impede the FeFET's development. Recently, the ultra-thin Al_2O_3 layer is found to be used as a tunnel switch for polarization reversal in ferroelectric Pb($Zr_{0.4}Ti_{0.6}$)O_3/ Al_2O_3 stacking layers, where Al_2O_3 layer is conductive during domain switching but restores to a high insular after the completion of polarization reversal [26]. Likewise, once the ferroelectric layer is replaced by an antiferroelectric, i.e., the dipoles with adjacent molecular/atomic layers are antiparallel, Al_2O_3 layer is highly conductive under a high enough field, and the antiparallel dipoles are switched into

the same direction, which is defined as the field-induced antiferroelectric (AF) into ferroelectric (FE) phase transition. As the external field is reduced below a backward coercive field, the field-induced ferroelectric phase switches back into the previous antiferroelectric state. However, within $Pb(Zr_{0.4}Ti_{0.6})O_3/Al_2O_3$ stacking layers the Al_2O_3 layer restores its previous insulation immediately to impede the phase switching due to the trapped interfacial charges. Therefore, the high-field ferroelectric phase is maintained in the AF/Al_2O_3 bilayer. Meantime, a depolarization field equal to the FE-AF backward coercive field is generated across Al_2O_3. The direction of the depolarization field can be changed with the polarization reversal of the high-field ferroelectric phase, which is useful to modulate the electron potential of the carriers within the conductive channel of the underlying silicon with the structure of AF-FET to realize a large on/off switching current ratio. Expectedly, the depolarization field in AF-FET is smaller than that in FeFET, which efficiently improves the ultimate data retention of the memory. However, the experimental work on this antiferroelectric structure is still unreported.

In this article, we show polarization-voltage (*P-V*) hysteresis loops and remanent polarization of Au/$Pb(Zr_{0.96}Ti_{0.04})O_3/Al_2O_3$/Pt stacking capacitors with different Al_2O_3 layer thicknesses for the confirmation of the stabilization of high-field ferroelectric phase in antiferroelectric $Pb(Zr_{0.96}Ti_{0.04})O_3$ after the removal of the external electric field. Next, we pattern this structure onto the top of the n-type Si to integrate AF-FETs. Finally, the capacitance-voltage (*C-V*) loops with different sweeping voltages are used to characterize the memory window and long-term data retention.

2 Experiments

The ultrathin Al_2O_3 layers were deposited onto both n-type (100) Si and Pt (111)/Ti/SiO_2/n-Si (100) substrates by atomic layer deposition (ALD) technique at 300°C. The base pressure of the chamber is 1.5 Torr. The ALD cycles for depositing the Al_2O_3 film were set to a certain number to achieve the final film thickness of 4–14 nm. The film thickness was measured using a Sopra GES5 Evolution spectroscopic ellipsometer. After that, the $Pb(Zr_{0.96}Ti_{0.04})O_3$ (PZT) thin films were formed through a Sol-Gel method on top of the Al_2O_3 layer. For the film deposition, $Pb(OCOCH_3)_2 \cdot 3H_2O$ was dissolved in methanol and refluxed for 2 h at 70°C. Separately, a mixture of $Zr(OC_3H_8)_4$ and $Ti(OC_4H_9)_4$ was dissolved into acetic acid and methanol, and the resulting solution was stirred at room temperature for 2 h. The based solutions with the Pb/Zr/Ti composition of 1.2:0.96:0.04 were mixed and refluxed for 3 h at 80°C. The PZT precursor contains the 20% Pb excess for the compensation of the volatile PbO during sintering. The PZT precursor was spin-coated onto Al_2O_3/n-Si (100) and Al_2O_3/Pt (111)/Ti/SiO_2/n-Si (100) substrates at 3,000 r.p.m. for 30 s, and the films were dried at 200°C for 30 s for the solvent volatilization.

As-prepared films were crystallized through a rapid thermal annealing (RTA) process at 650°C for 5 min at the atmosphere in order to form a perovskite structure. The circular Au top electrodes with the diameter of 200 μm were deposited through a shadow mask on PZT films through dc magnetron sputtering. All the samples were annealed at 400°C for 200 s after sputtering for the strengthening of the electrode adhesion.

P-V hysteresis loops were performed on a Radiant Technologies Materials Precision Analyzer with a triangular wave form of 1 kHz. *C-V* characteristics were measured using an Agilent E4980A precision LCR meter at 100 kHz with the amplitude of 0.05 V.

3 Results and discussion

Figure 1 shows the X-ray diffraction (XRD) patterns obtained for PZT thin films deposited on Pt (111)/Ti/SiO_2/n-Si (100) and Al_2O_3 (14 nm)/Pt (111)/Ti/SiO_2/n-Si (100) substrates, respectively. Both PZT films were well crystallized into a perovskite structure. As to the Al_2O_3/PZT bilayer, the preferred orientation for the PZT film on a Pt (111)/Ti/SiO_2/Si substrate has changed from (020)/(200) into (021)/(201).

Figure 2 (a) shows *P-V* hysteresis loops for PZT thin films (150 nm) with different thicknesses of Al_2O_3 layers (0, 7.5, and 14 nm) at room temperature. The *P-V* hysteresis

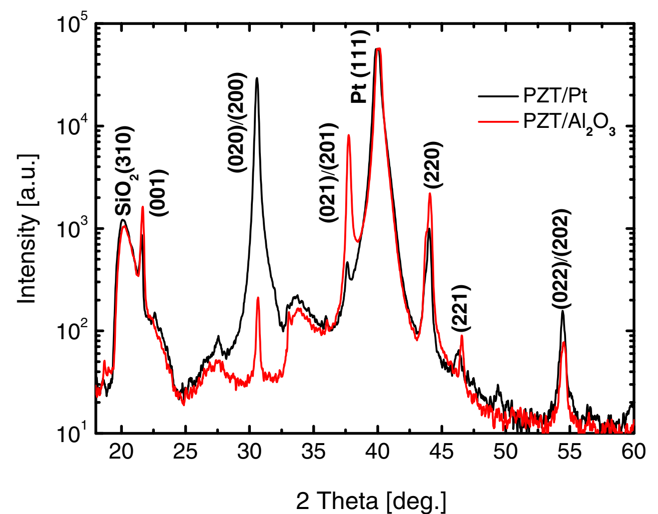

Fig. 1 The indexed XRD patterns for PZT thin films grown on Pt (111)/Ti/SiO_2/n-Si (100) and Al_2O_3 (14 nm)/Pt (111)/Ti/SiO_2/n-Si (100) substrates, respectively

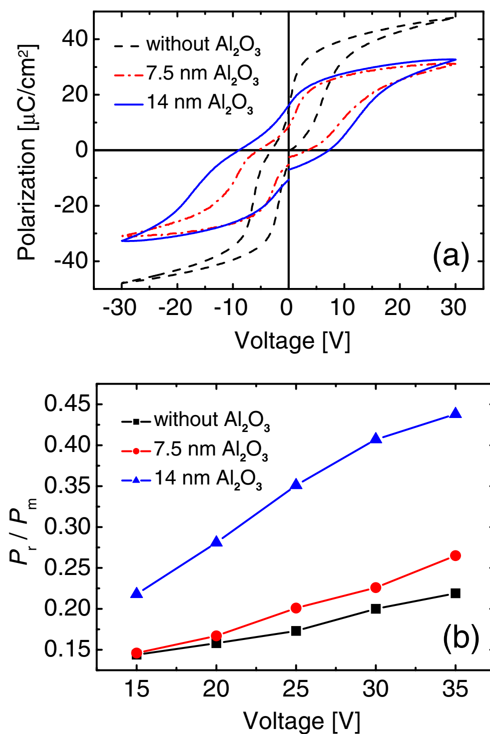

Fig. 2 (**a**) *P-V* hysteresis loops at 1 kHz for PZT (150 nm)/Al_2O_3 bilayers with different Al_2O_3 layer thicknesses at room temperature (**b**) The applied voltage dependence of the ratio of remanent polarization over maximum polarization (P_r/P_m) with different Al_2O_3 layer thicknesses at room temperature

loop of PZT without the Al_2O_3 layer shows a typical antiferroelectric behavior with a small remanent polarization (P_r). As integrated with the Al_2O_3 layer, the P_r value enlarges with the thickening of the Al_2O_3 layer from 7.5 to 14 nm, accompanied with the reduction of the maximum polarization at the highest voltage. This predicts the enhanced volume fraction of the stabilized ferroelectric phase with the inlaid Al_2O_3 layer.

Figure 2 (b) shows the voltage dependence of the ratio of the remanent polarization over the maximum polarization (P_m). The P_r/P_m ratio increases with enhanced voltage, and the P_r value is nonzero even in a pure antiferroelectric, which is due to the charge injection under the high field to temporally stabilize the ferroelectric phase. Once the injected charges are self-driven out of the film thickness by the internal field during the relaxation time, a previous antiferroelectric state is restored [27]. Likewise, the charge injection into the film is more effective within PZT/Al_2O_3 stacking layers under an enhanced voltage, where Al_2O_3 is conductive during domain switching. The injected charge density depends on the applied voltage. However, Al_2O_3 becomes an insulator again with the reduction of the field strength, and the injected charge is hardly driven out of the film thickness due to the Al_2O_3 blocking layer. Therefore, the high-field ferroelectric phase is stabilized into zero external field, and the P_r/P_m ratio increases with the Al_2O_3 layer thickness as well as with the enhancement of the applied voltage. The P_r/P_m ratio with Al_2O_3 thickness of 14 nm can reach 44% at 35 V, which is much higher than 21% without the Al_2O_3 layer. The significant enhancement of the P_r/P_m ratio indicates the importance of the optimum Al_2O_3 layer thickness on the stabilization of ferroelectric domains.

The injection current across the Al_2O_3 layer must be nonlinear with an exponential dependence of the applied field, such as for the F-N tunneling [26]. If the Al_2O_3 layer is too thin, the locked-in charge is leaky off with time. In this sense, the thicker Al_2O_3 layer is better to maintain the charge for a long time to keep a large remanent polarization. Nevertheless, the Al_2O_3 layer thickening requires a higher writing voltage for the memory to open the Al_2O_3 conductive channel for the completion of the AF-FE transition.

Ferroelectric retention of the PZT/Al_2O_3 (14 nm) bilayer was measured at room temperature using a PUND method from a Radiant Technology Precision analyzer. The testing pulse sequence used for retention is as follows: Firstly, a preset pulse of 30 V with the width of 1 ms was applied to write the domains; after a retention time, the ferroelectric polarization was read by applying two pulses with opposite polarities but the same absolute voltage value. Figure 3 shows the time dependence of the polarization, where P^* is the switched polarization between two opposite pulses and P_r is the remanent polarization. After retention time of 2×10^4 s, the polarization loss was only about 3%, clearly indicating the high-field ferroelectric phase maintained after the removal of the external field for a long time.

To reduce the writing voltage, the PZT and Al_2O_3 layer thicknesses are both reduced properly for the integration of AF-FETs. Figure 4 shows *C-V* loops at 100 kHz for Au/PZT (50 nm)/Al_2O_3 (6.3 nm)/n-Si (100) capacitor with a clockwise sweeping direction under different sweeping

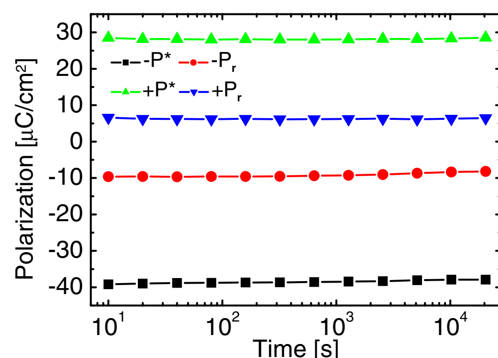

Fig. 3 Time dependence of the polarization from PUND measurements for PZT (150 nm)/Al_2O_3 (14 nm) bilayers at room temperature

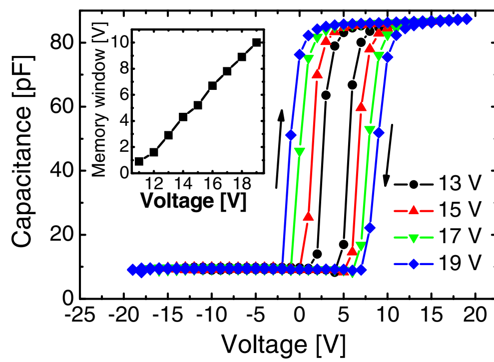

Fig. 4 *C-V* curves of Au/PZT (50 nm)/Al_2O_3 (6.3 nm) /n-Si (100) transistors under different sweeping voltages at room temperature. The insert shows the memory window as a function of sweeping voltage

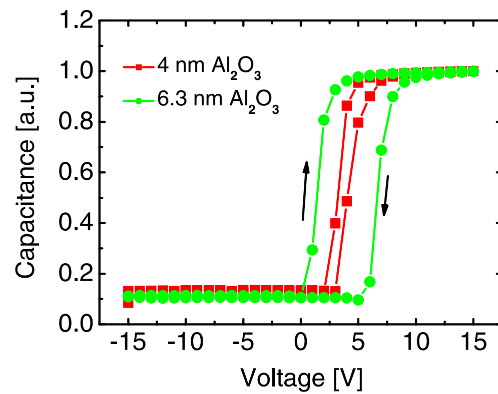

Fig. 5 *C-V* curves of Au/PZT (50 nm)/Al_2O_3 /n-Si (100) capacitors with different Al_2O_3 layer thicknesses

voltages. The loop exhibits a high/low capacitance ratio over 8:1 with the capacitance C given by the formula

$$C = \left(\frac{1}{C_{AF}} + \frac{1}{C_I} + \frac{1}{C_S}\right)^{-1}, \tag{1}$$

where

$$C_{AF} = \frac{A_{AF}\varepsilon_{AF}\varepsilon_0}{d_{AF}}, \tag{2}$$

$$C_I = \frac{A_I\varepsilon_I\varepsilon_0}{d_I}, \tag{3}$$

$$C_S = \left|\frac{\partial Q_S}{\partial \varphi_S}\right|, \tag{4}$$

C_{AF} is the capacitance of the antiferroelectric film, C_I is the capacitance of the insulating layer, C_S is the capacitance of the semiconductor, d_{AF} and d_I are the film thickness of the antiferroelectric and the insulator layers, respectively, $\varepsilon_{\rm AF}$ and ε_I are corresponding dielectric constants, A_{AF} and A_I are the areas of the antiferroelectric film and the insulator layer ($A_{AF} = A_I$), respectively, Q_S is the surface charge density of the semiconductor, and φ_S is the surface potential. From these loops, we determined the memory window under each sweeping voltage, as shown by the inset. The memory window increases with increasing applied voltage due to the enhanced injected charge density and fraction of stabilized ferroelectric phase. For the Al_2O_3 layer of 6.3 nm thickness, the memory window varies almost linearly from 2.9 to 10 V with the increasing voltage from 13 to 19 V without obvious saturation. This is because the applied voltage drop across the PZT film is not large enough to drive all the AF-FE phase switching. The switched domain fraction increases with the enhanced applied voltage due to the forward coercive-voltage distribution of the antiferroelectric over the voltage, and the effective field E_{AF} applied to the antiferroelectric layer is [28]

$$E_{AF} = \left(\frac{\varepsilon_I}{\varepsilon_{AF}d_I + \varepsilon_I d_{AF}}\right)(V_G - \varphi_S), \tag{5}$$

where V_G is the gate voltage on top electrode. The memory window is related to the ferroelectric coercive field with the form [29]

$$\Delta V_{window} \approx 2d_{AF}E_c + 2d_I E_{th}, \tag{6}$$

where E_{th} is the field across Al_2O_3 during domain switching. Since E_c has a distribution over the field, the memory window increases with the applied voltage. As V_G>20 V, the capacitor is completely damaged. Therefore, the data above 20 V are lost in the present investigation.

Figure 5 shows *C-V* curves of the above AF-FETs with the reduced Al_2O_3 layer thickness to 4 nm, whereas the PZT film thickness is fixed at 50 nm. The memory window with sweeping voltage between −15 to +15 V is 0.9 V, significantly smaller than 5.2 V with d_I=6.3 nm. This is

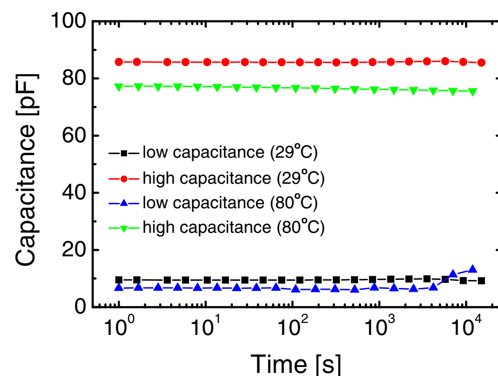

Fig. 6 Time dependences of high and low capacitances at 3 V for Au/PZT (50 nm)/Al_2O_3 (6.3 nm)/n-Si (100) transistors at different temperatures after a writing pulse of ±19 V for 1 s

believed that the Al_2O_3 layer is too thin to stabilize the high-field ferroelectric phase. Therefore, the maximum ratio of d_{AF}/d_I should be smaller than 12.5 in the stacking layer to achieve a large memory window.

The long-term data retention of the Au/PZT (50 nm)/ Al_2O_3 (6.3 nm)/n-Si (100) capacitor is shown in Fig. 6 at different temperatures. After the writing pulse of ±19 V with the width of 1 s, the time dependences of the high and low capacitances were measured continuously at the biasing voltage of 3 V. As seen from Fig. 6, the retention losses of the high and low capacitances are only about 0.3% and 2.7% at room temperature after 4 h. Either, the data retention loss at 80°C is below 11.4% after 12,000 s. Careful study of the retention loss at 80°C shows that the loss is caused by the electrical damaging of the capacitor under a long-time voltage stressing. It is believed that the intrinsic high-field ferroelectric domains are stable for maintaining of a good polarization retention.

4 Conclusion

In summary, we fabricated antiferroelectric PZT and high-k Al_2O_3 bilayers. *P-V* hysteresis loops and *C-V* curves demonstrate that the high-field ferroelectric phase within PZT can be stabilized at zero external field with an appropriate two-layer thickness ratio. The stabilized ferroelectric phase can generate a high depolarizing field to modulate the drain-source current in AF-FETs. A large memory window of 10 V was achieved for the PZT (50 nm)/Al_2O_3 (6.4 nm) bilayer under a writing voltage of 19 V. Consequent retention measurement shows the better performance of the transistor than the traditional FeFET for the memory application. It is believed that writing voltage can be reduced again with the shrinkage of both antiferroelectric and oxide layer thicknesses in the future.

Acknowledgments This work was supported by National Natural Science Foundation of China (No. 60776054), Shanghai Key Program (No. 08JC1402100 and No. 1052 nm07600), and the Program for Professor of Special Appointment (Eastern Scholar) at Shanghai.

References

1. J.F. Scott, C.A. Paz de Araujo, Science **246**, 1400 (1989)
2. C.A. Paz de Araujo, J.D. Cuchiaro, L.D. McMillan, M.C. Scott, J. F. Scott, Nature (London) **374**, 627 (1995)
3. H. Ishiwara, Mater. Res. Soc. Symp. Proc. **748**, 297 (2003)
4. H. Ishiwara, J. Semicond. Sci. Technol. **1**, 1 (2001)
5. E. Tokumitsu, R.I. Nakamura, H. Ishiwara, IEEE Electron. Device. Lett. **18**, 160 (1992)
6. S. Mathews, R. Ramesh, T. Venkatesan, J. Benedetto, Science **276**, 238 (1997)
7. J.H. Jung, S.B. Hong, H.S. Park, United States Patent No. 20050133841 A1 (23 June 2005)
8. M. Takahashi, K. Kodama, T. Nakaiso, M. Noda, M. Okuyama, Jpn. J. Appl. Phys. **40**, 2923 (2001)
9. M. Lim, T.S. Kalkur, Integr. Ferroelectr. **14**, 247 (1997)
10. C.H. Ahn, J.M. Triscone, N. Archibald, M. Decroux, R.H. Hammond, T.H. Geballe, F. Fischer, M.R. Beasley, Science **269**, 373 (1995)
11. T.P. Ma, J.P. Han, IEEE Electron. Device Lett. **23**, 386 (2002)
12. A. Chin, M.Y. Yang, C.L. Sun, S.Y. Chen, IEEE Electron. Device Lett. **22**, 336 (2001)
13. K.H. Kim, J.P. Han, S.W. Jung, T.P. Ma, IEEE Electron. Device Lett. **23**, 82 (2002)
14. B.E. Park, H. Ishiwara, Inter. Ferroelectr. **62**, 141 (2004)
15. K. Aizawa, B.E. Park, Y. Kawashima, K. Takahashi, H. Ishiwara, Appl. Phys. Lett. **85**, 3199 (2004)
16. B.E. Park, K. Takahashi, H. Ishiwara, Appl. Phys. Lett. **85**, 4448 (2004)
17. K. Takahashi, K. Aizawa, B.E. Park, H. Ishiwara, Jpn. J. Appl. Phys. **44**, 6218 (2005)
18. S. Sakai, R. Ilangovan, IEEE Electron. Device Lett. **25**, 369 (2004)
19. Q.H. Li, S. Sakai, Appl. Phys. Lett. **89**, 222910 (2006)
20. T. Hirai, Y. Fujisaki, K. Nagashima, H. Koike, Y. Tarui, Jpn. J. Appl. Phys. **36**, 5908 (1997)
21. N.A. Basit, H.K. Kim, J. Blachere, Appl. Phys. Lett. **73**, 3941 (1998)
22. T.P. Juan, C.Y. Chang, J.Y. Lee, IEEE Electron. Device Lett. **27**, 217 (2006)
23. W.C. Shih, P.C. Juan, J.Y. Lee, J. Appl. Phys. **103**, 094110 (2008)
24. M.H. Tang, Y.C. Zhou, X.J. Zhang, Z. Ye, C.P. Cheng, Z.S. Hu, J. He, Inter. Ferroelectr. **94**, 105 (2007)
25. X.B. Lu, K. Maruyama, H. Ishiwara, J. Appl. Phys. **103**, 044105 (2008)
26. A.Q. Jiang, H.J. Lee, C.H. Kim, C.S. Hwang, Adv. Mater. **21**, 2870 (2009)
27. A.Q. Jiang, T.A. Tang, S. Corkovic, Q. Zhang, Appl. Phys. Lett. **93**, 212908 (2008)
28. S.K. Lee, Y.T. Kim, S. Kim, J. Appl. Phys. **91**, 9303 (2002)
29. T. Kanashima, M. Okuyama, Jpn. J. Appl. Phys. **38**, 2044 (1999)